Amendments to the Claims:

Claim 1 (previously presented): A quadrature amplitude modulation demodulator comprising a timing synchroniser for resampling an incoming sampled quadrature amplitude modulated signal and a controller for controlling said timing synchroniser, said timing synchroniser having an acquisition mode in which said incoming signal is resampled with a sampling period which sweeps between first upper and lower limit values at a plurality of different timing synchroniser sweep rates, said controller being arranged to initiate an acquisition cycle at a higher one of said timing synchroniser sweep rates, to reduce a timing synchroniser sweep rate monotonically and to switch said timing synchroniser to a tracking mode if a timing error is below a first threshold.

Claim 2 (previously presented): A demodulator as claimed in claim 1, in which said controller is arranged, in said acquisition mode, to repeat each of said timing synchroniser sweep rates a first predetermined number of times before selecting a next of said timing synchroniser sweep rates.

Claim 3 (original): A demodulator as claimed in claim 1, in which said controller is arranged, in said acquisition mode, to repeat said acquisition cycle a second predetermined number of times.

Claim 4 (original): A demodulator as claimed in claim 1, in which said controller is arranged to institute a shift in a frequency band of said incoming signal if said timing error remains above said first threshold after said acquisition cycle and to initiate a further acquisition cycle.

Claim 5 (original): A demodulator as claimed in claim 1, comprising an adaptive multipath equaliser connected to said timing synchroniser, said controller being arranged to disable adaption of said equaliser until said timing error falls below said first threshold.

Claim 6 (original): A demodulator as claimed in claim 5, in which said controller is arranged to initiate another acquisition cycle of said timing synchroniser if said equaliser is unable to complete adaption in a predetermined time period.

Claim 7 (original): A demodulator as claimed in claim 1, comprising a carrier synchroniser for locking a phase of a locally generated signal to a carrier of said incoming signal

Claim 8 (original): A demodulator as claimed in claim 5, comprising a carrier synchroniser for locking a phase of a locally generated signal to a courier of said incoming signal and in which said controller is arranged to disable said carrier synchroniser until said equaliser has completed adaption.

Claim 9 (previously presented): A demodulator as claimed in claim 7, in which said carrier synchroniser has an acquisition mode in which a frequency of a locally generated signal sweeps between second upper and lower limited values at a plurality of different carrier synchroniser sweep rates, said controller being arranged to initiate a carrier acquisition cycle at a higher one of said carrier synchroniser sweep rates, to reduce a carrier synchroniser sweep rate monotonically and to switch said carrier synchroniser to a tracking mode if a carrier synchronisation error is below a second threshold.

Claim 10 (previously presented): A demodulator as claimed in claim 9, in which said controller is arranged, in said carrier synchroniser acquisition mode, to repeat each of said carrier synchroniser sweep rates a third predetermined number of times before selecting a next of said carrier synchroniser sweep rates.

Claim 11 (original): A demodulator as claimed in claims 9, in which said controller is arranged, in said carrier synchroniser acquisition mode, to repeat said carrier acquisition cycle a fourth predetermined number of times.

Claim 12 (original): A demodulator as claimed in claim 9, in which said controller is arranged to return said carrier synchroniser to said acquisition mode if a mean square error of demodulated symbols remains above a third threshold for a predetermined time period.

Claim 13 (previously presented): A quadrature amplitude demodulator comprising a carrier synchroniser for locking a phase of a locally generated signal to a carrier of an incoming signal and a controller for controlling said carrier synchroniser, said carrier synchroniser having an acquisition mode in which a frequency of a locally generated signal sweeps between upper and lower limit values at a plurality of different carrier synchroniser sweep rates, said controller being arranged to initiate a carrier acquisition cycle at a higher one of said sweep rates, to reduce said sweep rate monotonically and to switch said carrier synchroniser to a tracking mode if a carrier synchronisation error is below a first threshold.

Claim 14 (previously presented): A demodulator as claimed in claim 13, in which said controller is arranged, in said acquisition mode, to repeat each of said sweep rates a predetermined number of times before selecting a next of said sweep rates.

Claim 15 (previously presented): A demodulator as claimed in claims 13, in which said controller is arranged, in said acquisition mode, to repeat said carrier acquisition cycle a predetermined number of times.

Claim 16 (previously presented): A demodulator as claimed in claim 13, in which said controller is arranged to return said carrier synchroniser to said acquisition mode if a mean square error of demodulated symbols remains above a second threshold for a predetermined time period.

Claim 17 (previously presented): A receiver comprising a quadrature amplitude modulation demodulator, the quadrature amplitude modulation demodulator including a timing synchroniser for resampling an incoming sampled quadrature amplitude modulated signal and a controller for controlling said timing synchroniser, said timing synchroniser having an acquisition mode in which said incoming signal is resampled with a sampling period which sweeps between first upper and lower limit values at a plurality of different sweep rates, said controller being arranged to initiate an acquisition cycle at a higher one of said sweep rates, to reduce said sweep rate monotonically and to switch said timing synchroniser to a tracking mode if a timing error is below a first threshold.

Claim 18 (currently amended): A receiver comprising a quadrature amplitude demodulator, the quadrature amplitude demodulator including a carrier synchroniser for locking a phase of a locally generated signal to a carrier of an incoming signal and a controller for controlling said carrier synchroniser, said carrier synchroniser having an acquisition mode in which a frequency of a locally generated signal sweeps between upper and lower limit values at a plurality of different sweep rates, said controller being arranged to initiate a carrier acquisition cycle at a higher one of said sweep rates, to reduce said sweep rate monotonically and to switch said carrier synchroniser to a tracking mode if a carrier synchronisation error is below a ~~second~~ first threshold.

Claim 19 (previously presented): A demodulator as claimed in claim 1, in which said controller is arranged to initiate said acquisition cycle for said timing synchronizer at a highest of said timing synchroniser sweep rates.

Claim 20 (previously presented): A demodulator as claimed in claim 9, in which said controller is arranged to initiate said carrier acquisition cycle at a highest of said carrier synchroniser sweep rates.

Claim 21 (previously presented): A demodulator as claimed in claim 13, in which said controller is arranged to initiate said carrier acquisition cycle at a highest of said sweep rates.

Claim 22 (previusly presented): A receiver as claimed in claim 17, in which said controller is arranged to initiate said acquisition cycle at a highest of said sweep rates.

Claim 23 (previously presented): A receiver as claimed in claim 18, in which said controller is arranged to initiate said carrier acquisition cycle at a highest of said sweep rates.

Claim 24 (previously presented): A quadrature amplitude modulation demodulator comprising a timing synchroniser for resampling an incoming sampled quadrature amplitude modulated signal

and a controller for controlling said timing synchroniser, said timing synchroniser having an acquisition mode in which said incoming signal is resampled with a sampling period which sweeps between first upper and lower limit values at a plurality of different timing synchroniser sweep rates, said controller being arranged to initiate an acquisition cycle at a first one of said timing synchroniser sweep rates, determining whether said timing synchroniser achieves a lock at a completion of a sweep between said upper and lower limit values at said first timing synchronizer sweep rate, selecting a different one of said timing synchroniser sweep rates if a lock is not achieved at said first timing synchroniser sweep rate, and switching said timing synchroniser to a tracking mode if a lock is achieved.

Claim 25 (previously presented): A demodulator as claimed in claim 24, further comprising a carrier synchroniser for locking a phase of a locally generated signal to a carrier of said incoming signal, in which said carrier synchroniser has an acquisition mode in which a frequency of a locally generated signal sweeps between second upper and lower limited values at a plurality of different carrier synchroniser sweep rates, said controller being arranged to initiate a carrier acquisition cycle at a first one of said carrier synchroniser sweep rates, determining whether said carrier synchroniser achieves a lock at a completion of a sweep between said upper and lower limit values at said first carrier synchronizer sweep rate, selecting a different one of said carrier synchroniser sweep rates if a lock is not achieved at said first timing synchroniser sweep rate, and switching said carrier synchronizer to a tracking mode if a lock is achieved.